

FIG.1

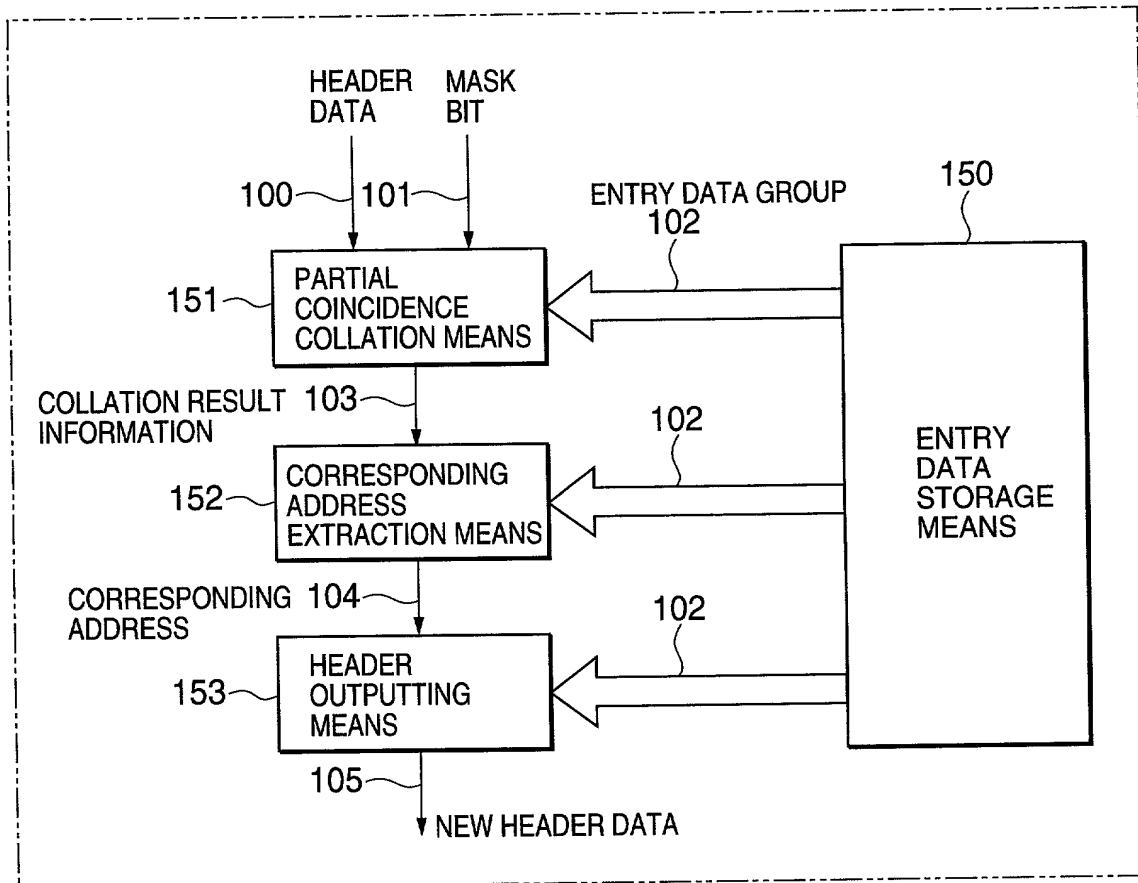
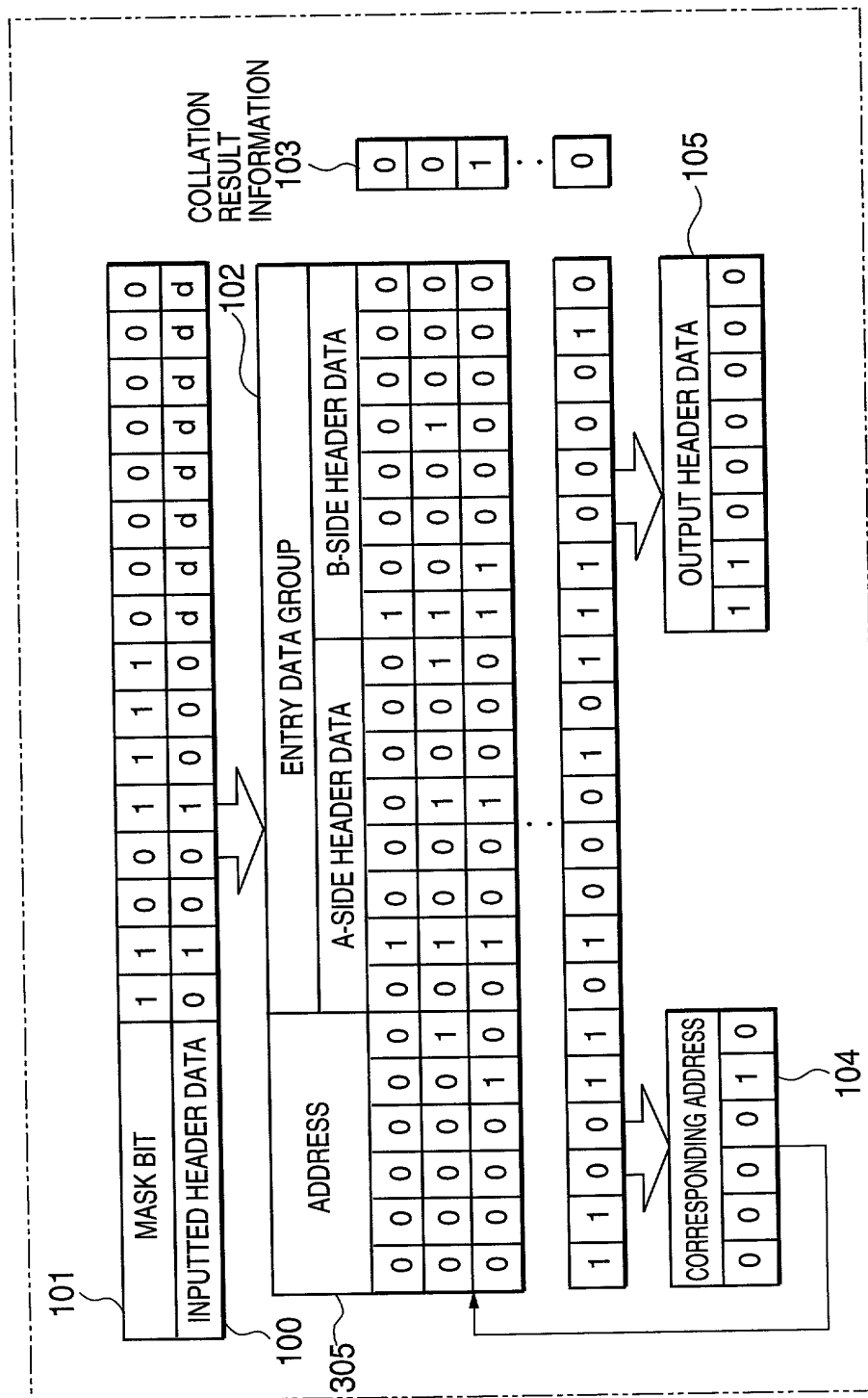


FIG.2



The diagram illustrates a data processing system 400. It begins with a MASK WORD (1) and INPUTTED HEADER DATA (0 1 0 0 1 0 0 0 d d d d d). These are combined to form an ENTRY DATA GROUP (100), which is divided into ADDRESS and ENTRY DATA. The ADDRESS is a 4-bit value (0 0 0 0). The ENTRY DATA is divided into A-SIDE HEADER DATA and B-SIDE HEADER DATA. The A-SIDE HEADER DATA is a 4-bit value (0 1 0 0). The B-SIDE HEADER DATA is a 4-bit value (1 0 0 0). The ADDRESS and A-SIDE HEADER DATA are combined to form a CORRESPONDING ADDRESS (0 0 0 0 1 0). This address is used to select data from a memory structure (104), which is a 4-bit value (0 0 0 0). The selected data is then combined with the B-SIDE HEADER DATA to form the OUTPUT HEADER DATA (1 1 0 0 0 0 0 0).

400

MASK WORD

1

0

INPUTTED HEADER DATA

0 1 0 0 1 0 0 0 d d d d d

100

ENTRY DATA GROUP

ADDRESS

0 0 0 0

A-SIDE HEADER DATA

0 1 0 0

B-SIDE HEADER DATA

1 0 0 0

104

CORRESPONDING ADDRESS

0 0 0 0 1 0

105

OUTPUT HEADER DATA

1 1 0 0 0 0 0 0

FIG.4

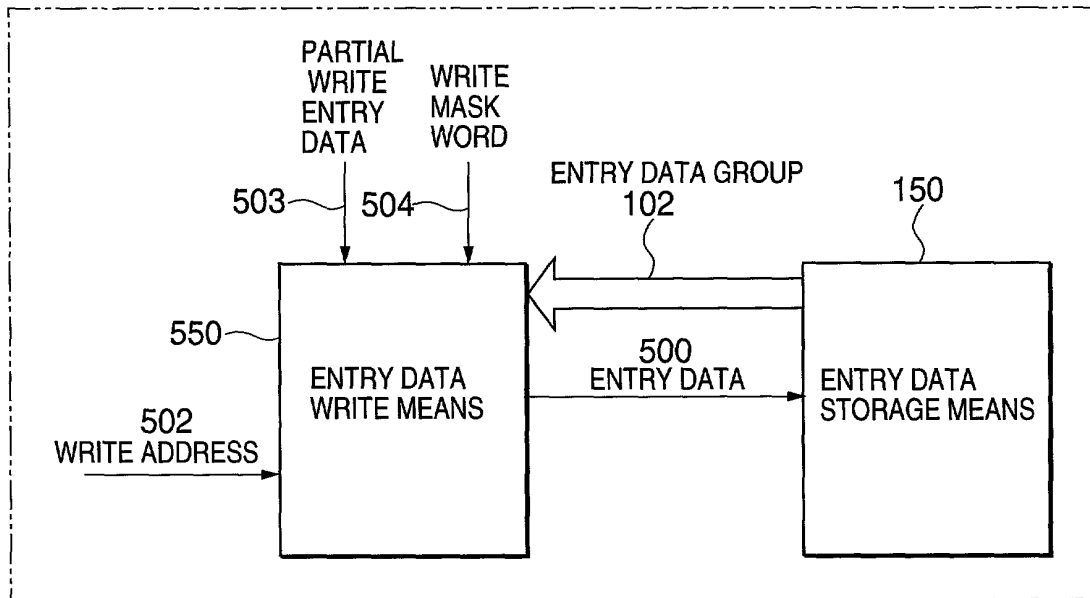


FIG.5

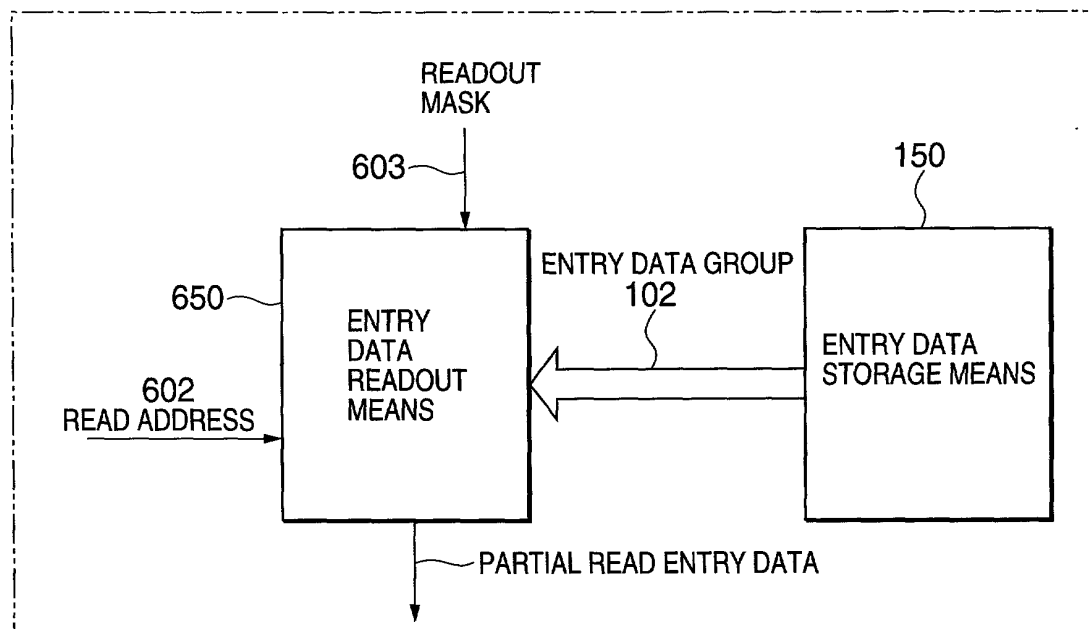


FIG.6

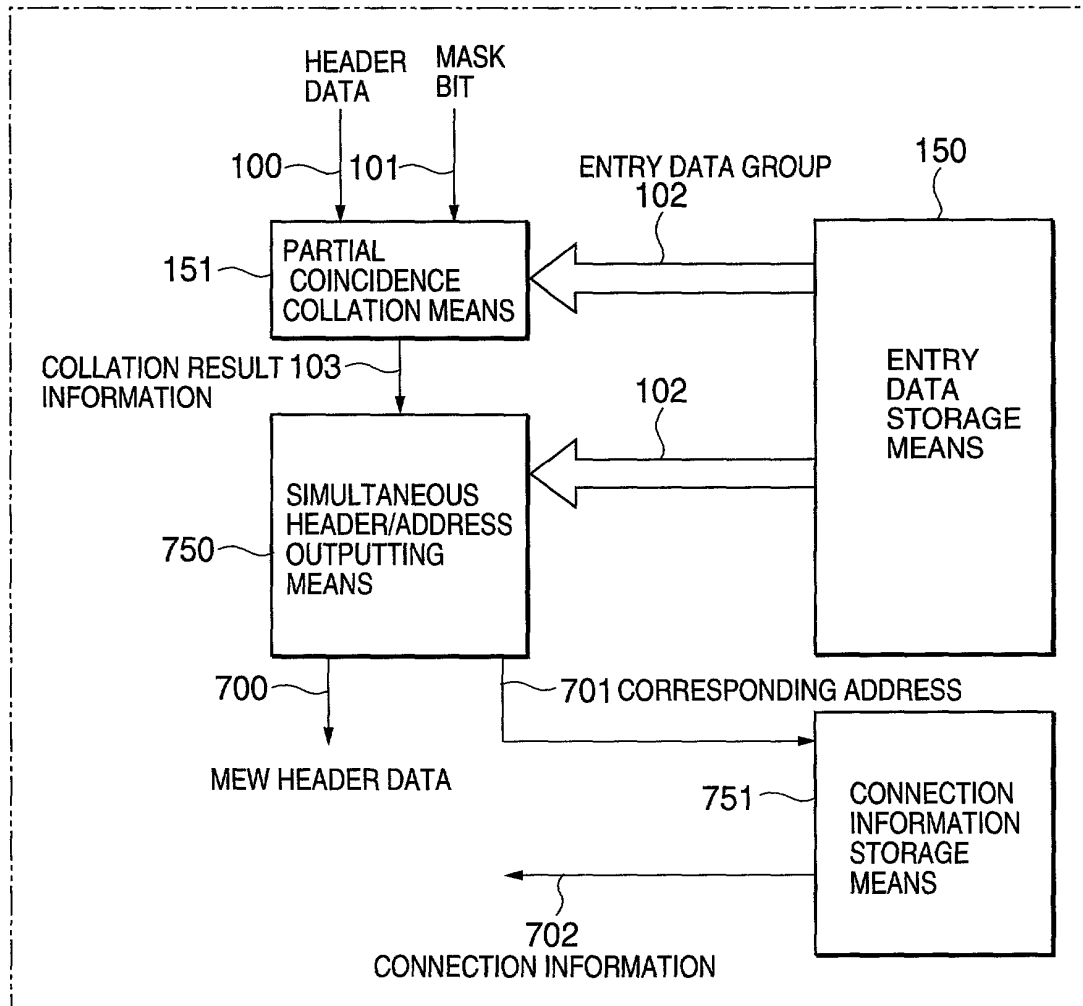


FIG.7

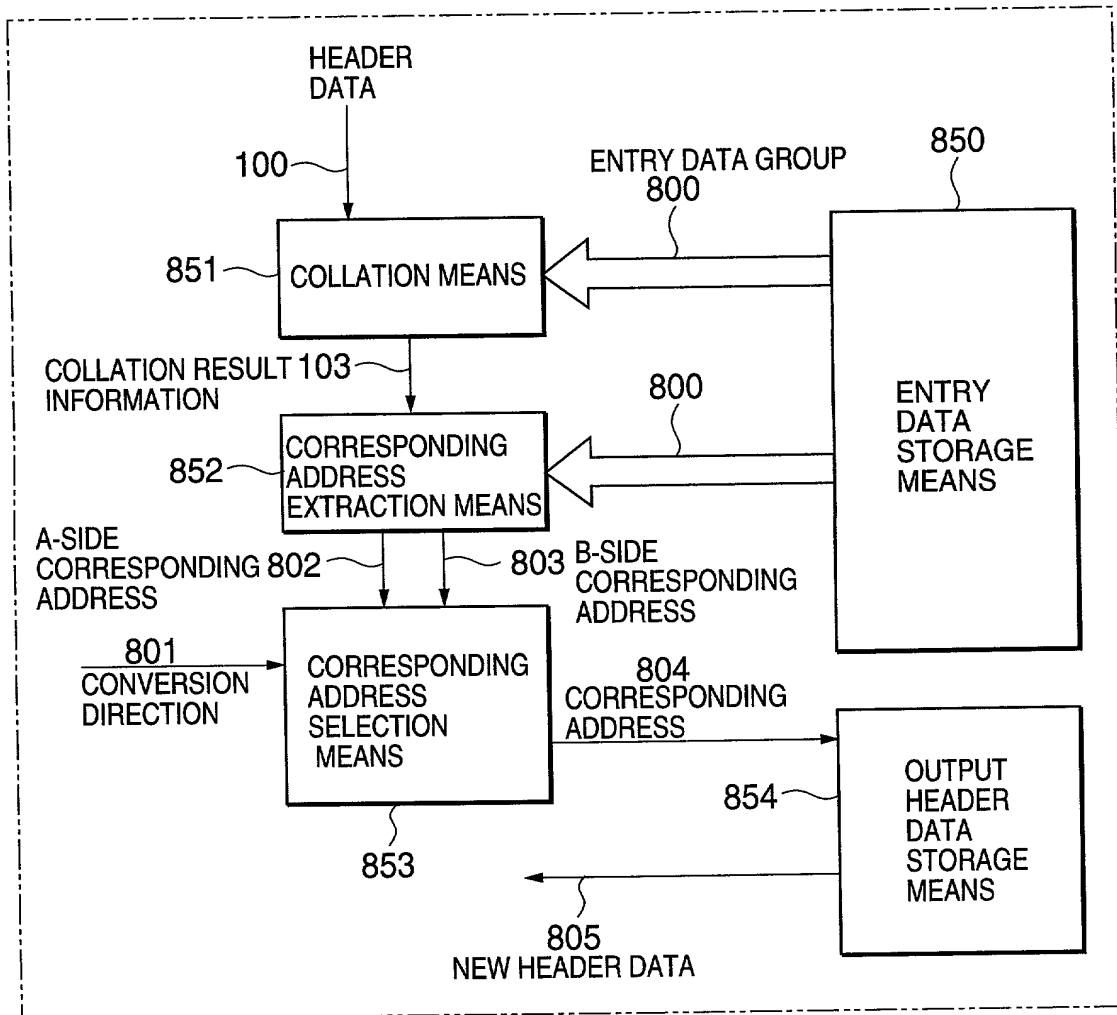


FIG.8

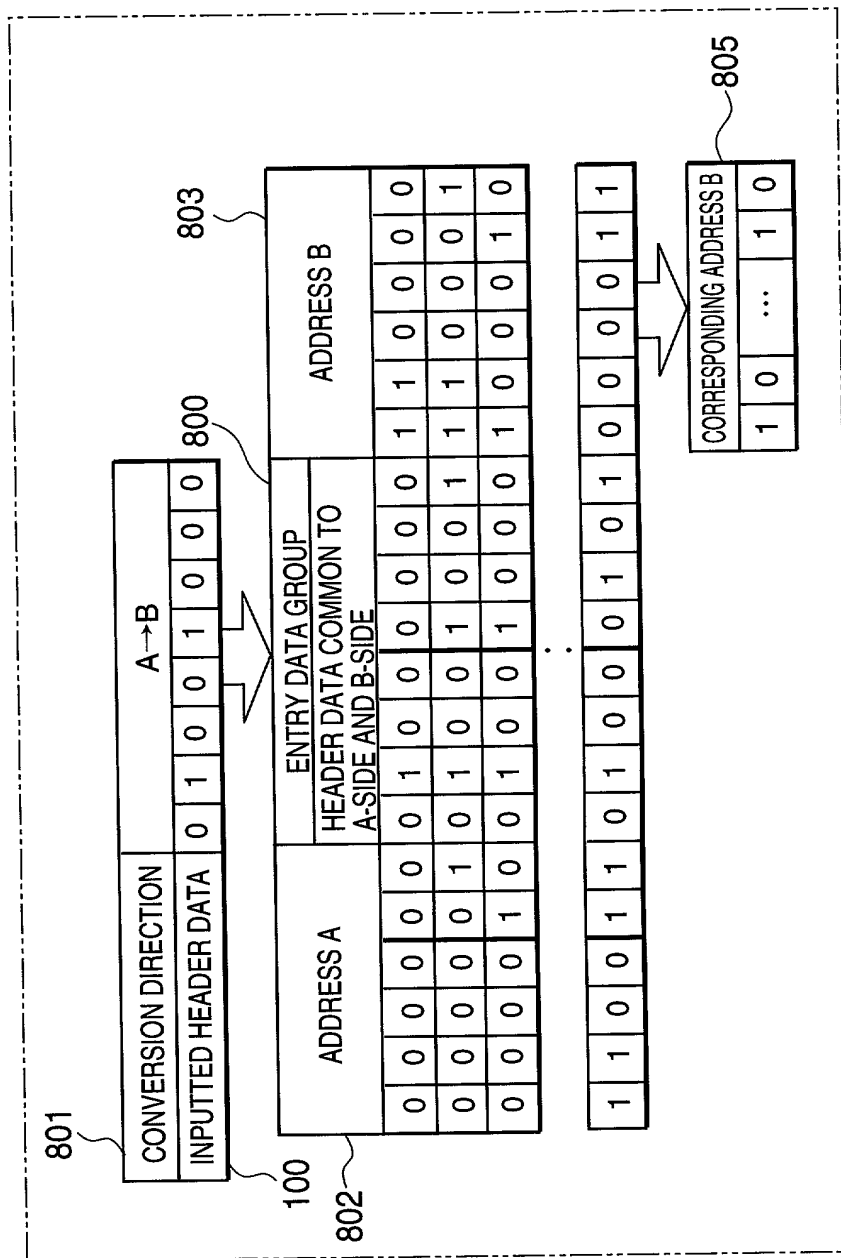


FIG.9

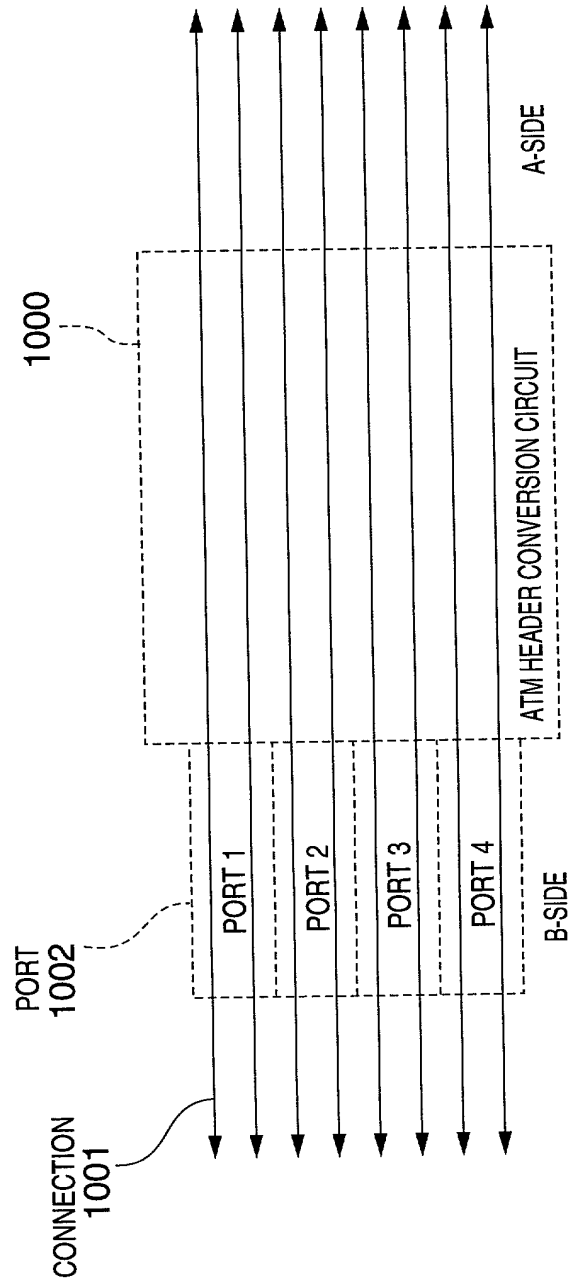


FIG.10

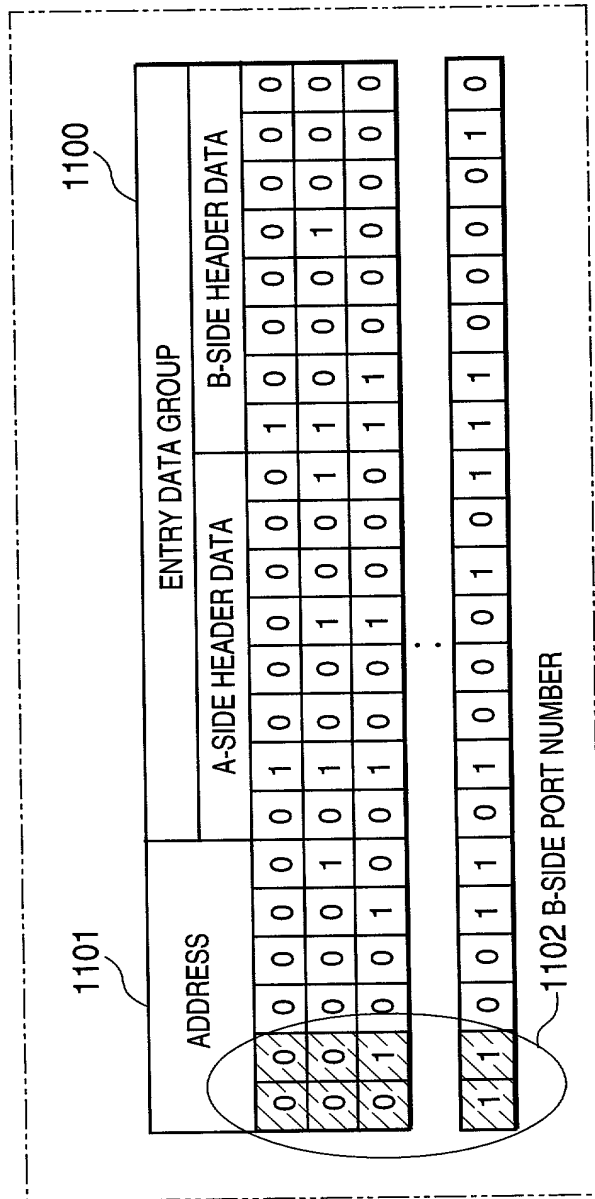


FIG.12

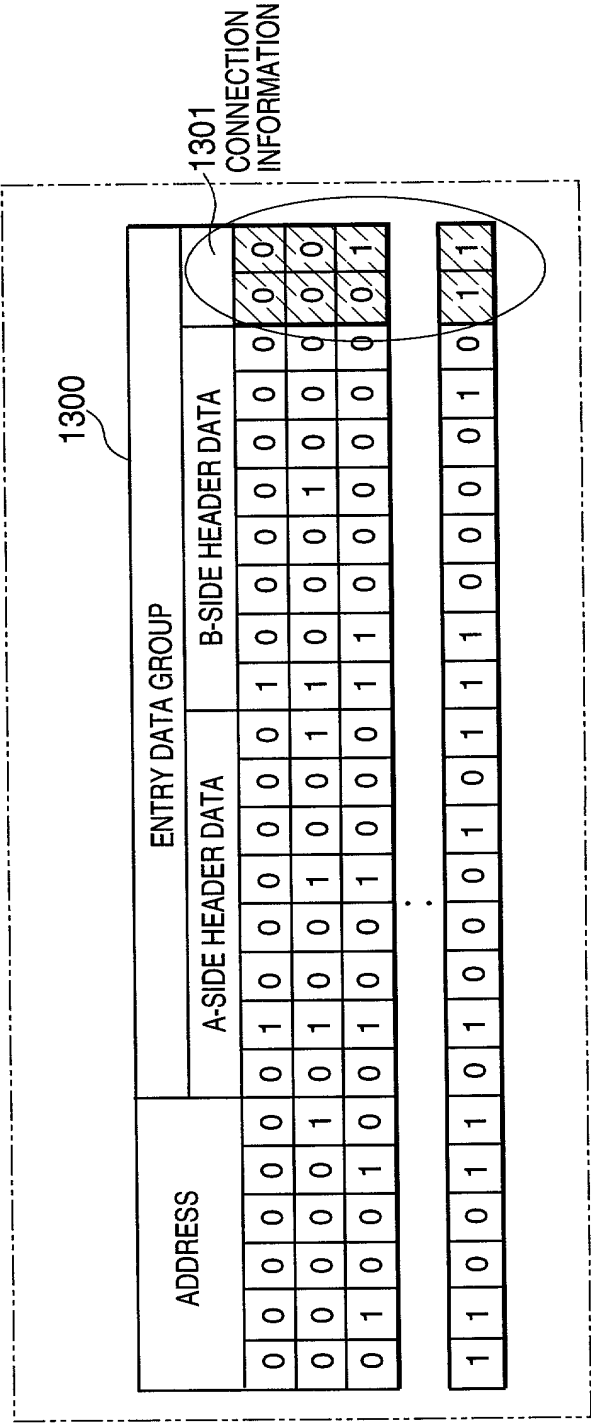


FIG.13

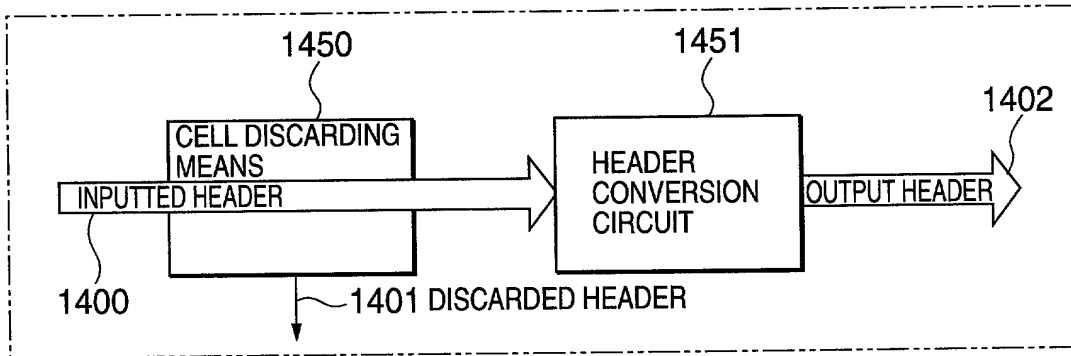


FIG.14

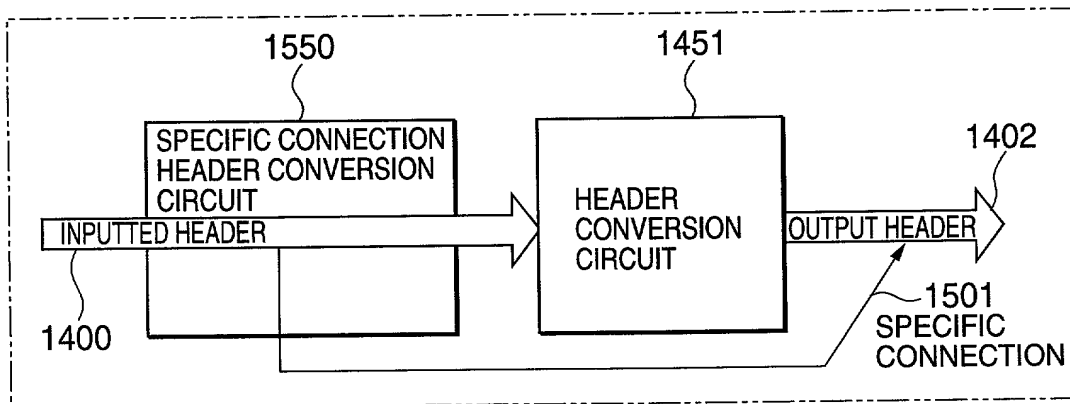


FIG.15

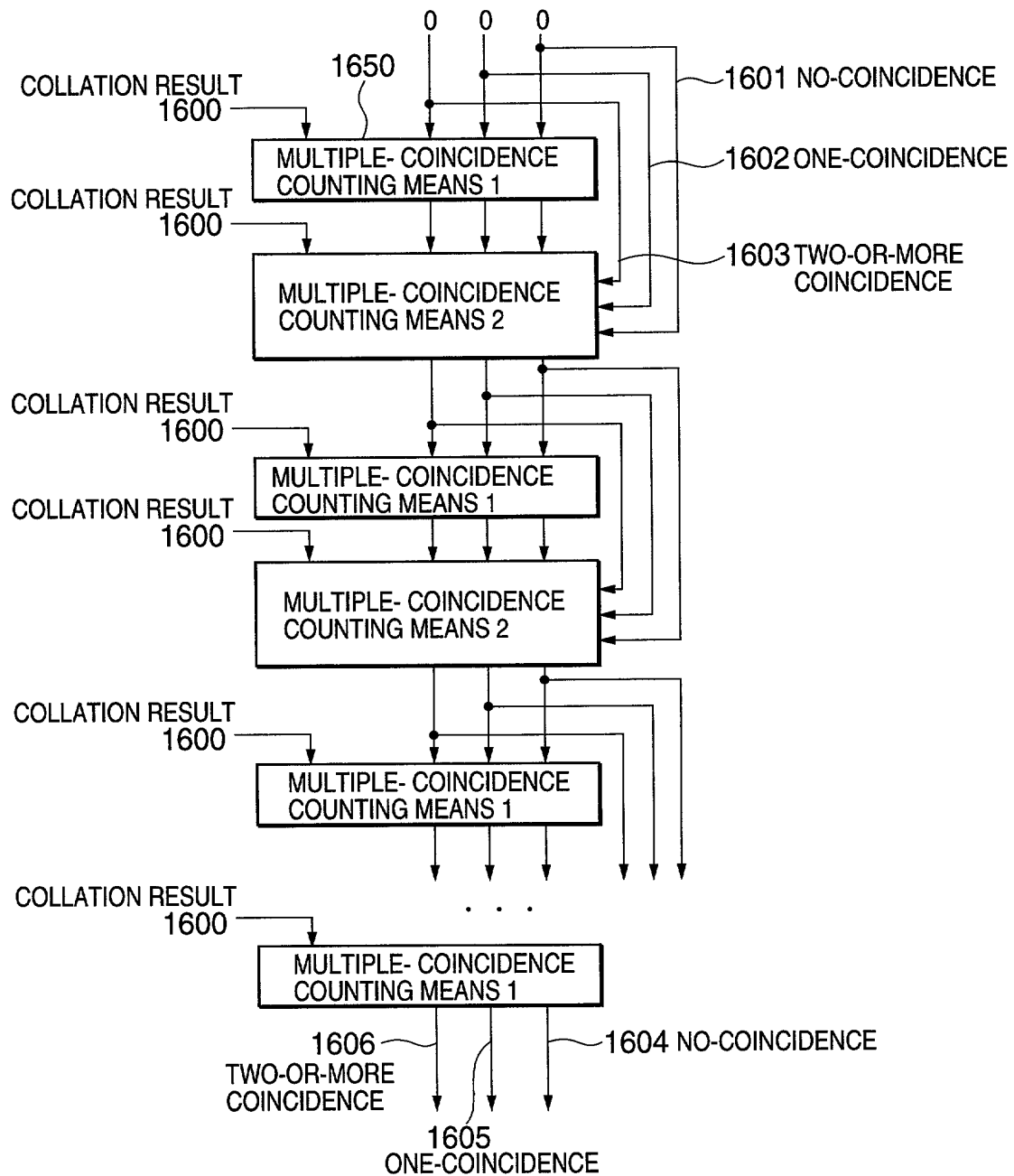


FIG.16A

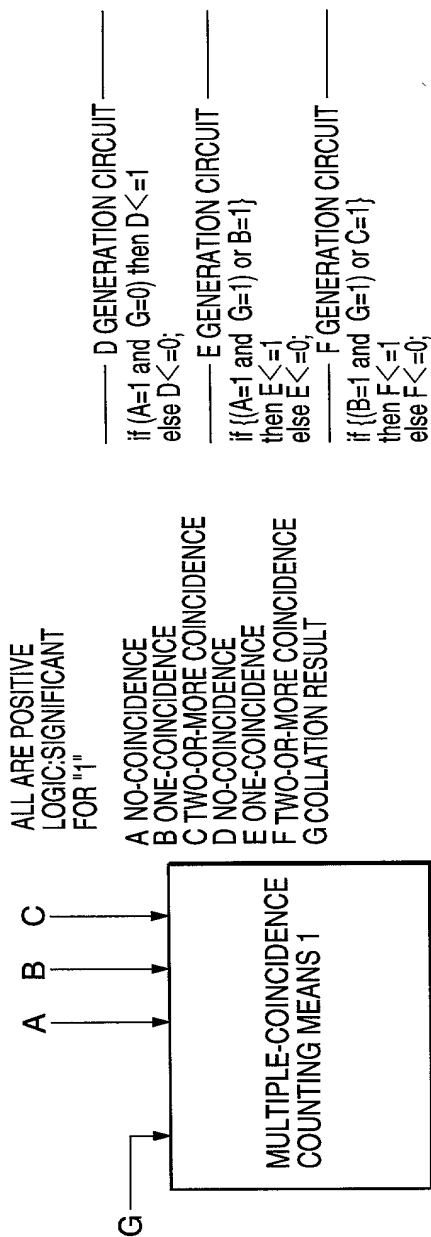


FIG.16B

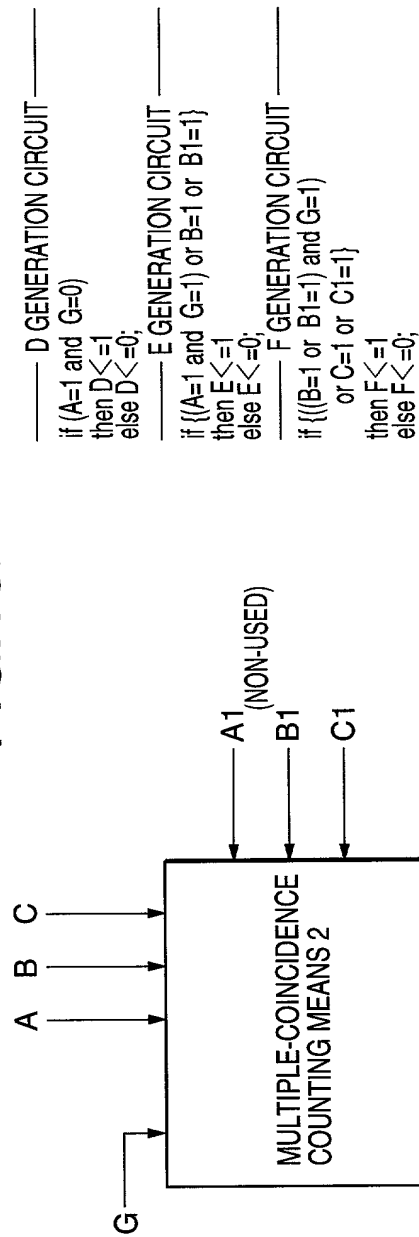


FIG.17

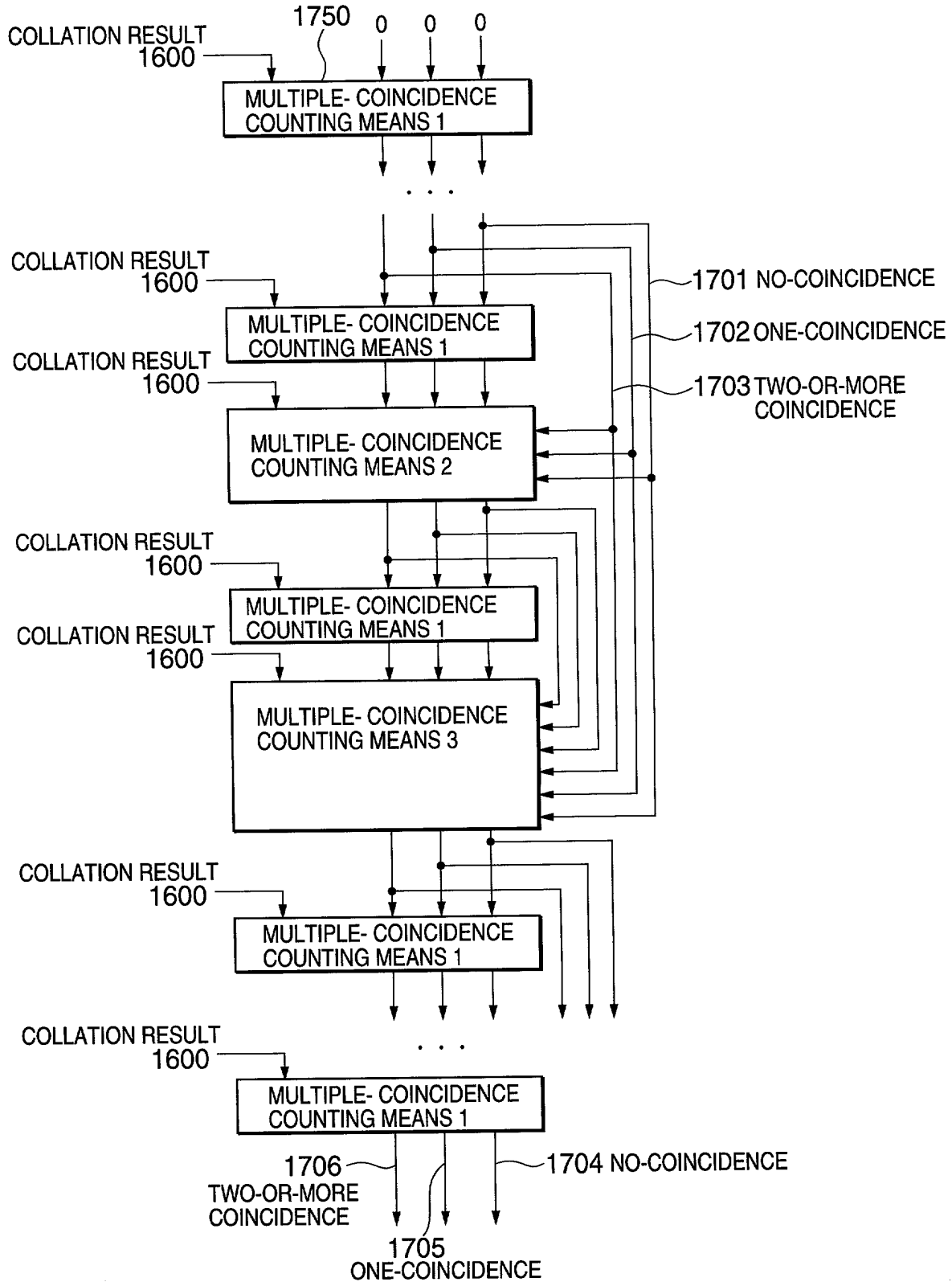


FIG.18

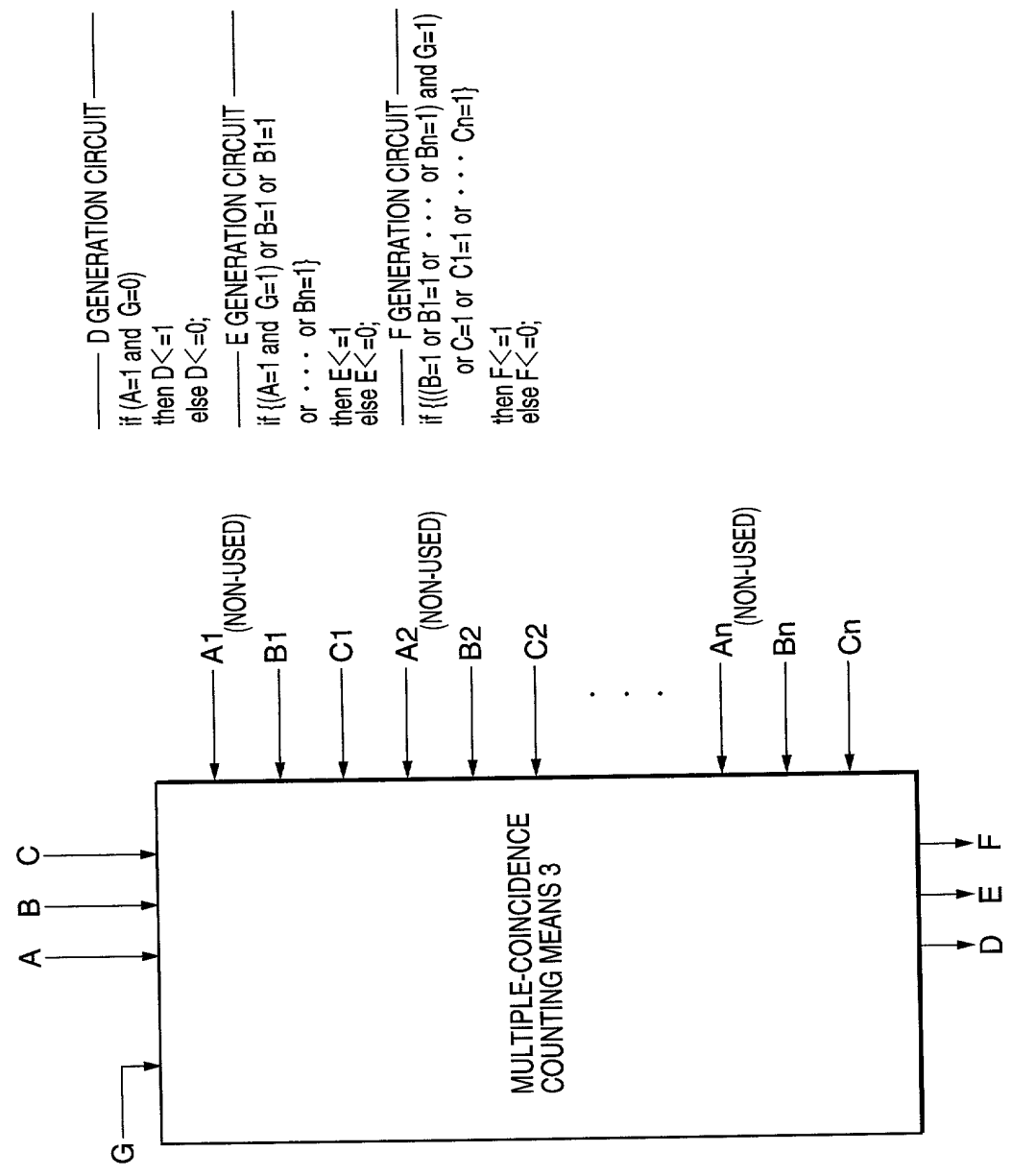


FIG.19
RELATED ART

